What Is Claimed Is:

1. A complementary metal oxide semiconductor (CMOS) semiconductor device, comprising:

a first gate electrode having a stacked structure of a first metal layer, a polysilicon layer and a second metal layer formed in a p-well region of a cell region and an n-well region of a peripheral circuit region; and

a second gate electrode having a stacked structure of the polysilicon layer and the second metal layer formed on a p-well of a peripheral circuit region.

2. The device of claim 1, wherein the first metal layer has a work function ranging from 4.8 eV to 5.0 eV.

3. The device of claim 1, wherein the first metal layer has a thickness ranging from 5 to 1000Å.

4. The device of claim 1, wherein the first metal layer comprises at least one metal layer selected from the group consisting of TiN, TiAlN, TiSiN, WN and TaN.

5. The device of claim 1, wherein the polysilicon layer have a thickness ranging from 10 to 1000Å.

6. The device of claim 1, wherein the second metal layer have a thickness ranging from 10 to 1000Å.

7. A method for manufacturing a complementary metal oxide semiconductor (CMOS) device, comprising:

forming a first metal layer on a p-well region of a cell region and a n-well region of a peripheral circuit region of a semiconductor substrate including a gate insulation film;

sequentially forming a polysilicon layer and a second metal layer on the entire upper surface of the semiconductor substrate; and

forming a first gate electrode having a stacked structure of a first metal layer pattern, a polysilicon layer pattern, and a second metal layer pattern on the p-well of the cell region and the n-well of the peripheral circuit region, and simultaneously forming a second gate electrode having a stacked structure of the polysilicon layer pattern and the second metal layer pattern on a p-well of a peripheral circuit region by etching the first metal layer, the second metal layer and the polysilicon layer via a photolithography process using a gate electrode mask.

8. The method of claim 7, wherein the gate insulation film has a thickness ranging from 5 to 100Å.

9. The method of claim 7, wherein the gate insulation film is an dielectric film.

10. The method of claim 9, wherein the dielectric film comprises Al_2O_3, HfO_2, $Hf \bullet SiO_2$, $Zr \bullet SiO_2$ or combination thereof.

11. The method of claim 7, wherein the first metal layer has a work function ranging from 4.8 eV to 5.0 eV.

12. The method of claim 7, wherein the first metal layer has a thickness ranging from 5 to 1000Å.

13. The method of claim 7, wherein the material forming the first metal layer comprises TiN, TiAlN, TiSiN, WN, TaN or combination thereof.

14. The method of claim 7, wherein the polysilicon layer has a thickness ranging from 10 to 1000Å.

15. The method of claim 7, wherein the second metal layer has a thickness ranging from 10 to 1000Å.

16. The method of claim 7, wherein etching process of the first metal layer is a wet etching process using a solution selected from the group consisting of piranha, SC-1, and SC-2, and a mixture thereof.

17. A method for manufacturing a complementary metal oxide semiconductor (CMOS) device, comprising:

forming a photo resist film pattern on a semiconductor substrate including a gate insulation film, the photo resist film exposing a p-well region of a cell and an n-well region of a peripheral circuit region;

forming a first metal layer having a work function ranging from 4.8 to 5.0eV on the entire surface of the semiconductor substrate;

removing the photo resist film pattern to expose the p-well region of the peripheral circuit region including the gate insulation film;

sequentially forming a polysilicon layer and a second metal layer on the entire surface of the semiconductor substrate;

forming a first gate electrode having a stacked structure of a first metal layer pattern, a polysilicon layer pattern, and a second metal layer pattern on the p-well of the cell region and the n-well of the peripheral circuit region, and simultaneously forming a second gate electrode having a stacked structure of the polysilicon layer pattern, a second metal layer pattern on a p-well of a peripheral circuit region by etching the first metal layer, the second metal layer and the polysilicon layer via a photolithography process using a gate electrode mask; and

forming an n-type source/drain region by ion-implanting n-type impurities into the P-well; and

forming a p-type source/drain region by ion-implanting p-type impurities into the n-well.